UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,803	12/29/2000	Wolfgang Roesner	AUS920000227US1	5327

42640 7590 12/05/2005

DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HWY
SUITE 2110
AUSTIN, TX 78759

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,803	ROESNER ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-10 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1,2,4-6,8-10, 12-15 were examined.

1a. Claims 3,7,11 were cancelled.

Section I: Prosecution Reopened

2. In view of the appeal brief filed on 7/15/05, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2). Reopening is necessitated based on applicants' argument in the brief. Based on applicants' brief and interpretation, examiner has provided new art and looks forward to advancing prosecution.

Section II: Non-Final Rejection (3rd Office Action)

Joint Inventors Common Ownership Presumed

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims1,2,4-6,8-10,12-15 are rejected under 35 U.S.C. 103 (a) as obvious by Wu et al., ("Digital PWM Control: Application in Voltage Regulation Modules") (hereafter

Wu) in view of Improv Systems Inc. (hereafter Improv) and in further view of Bargh et al., (US Patent 6,223,142 (2001)) (hereafter Bargh). Wu teaches signal overrides within a HDL simulation, it fails to teach post-compilers. Improv teaches HDL simulation with post-compilers but fails to teach instantiation, insertion of comments within the HDL and port mapping. Bargh not only teaches HDL simulation but also teaches instantiation, insertion of comments within the HDL and port mapping, but also doesn't teach post-compiler nor signal overrides.

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Wu by way of Bargh and Improv to provide improved efficiency and accuracy in identifying failures; assess the logical correctness of the overall model (Bargh: column 3, lines 52-55) as well as to provide a need for complex multi-functional systems (Improv: pg.3).

Claim 1. In a computer-aided design and verification system a method for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL) , said method comprising: instantiating (Bargh: column 7, lines 55-59) an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax (Bargh: column 27, lines 38-40) , said non-conventional HDL comment processed by a post-complier model build process, wherein said non-conventional load tool instantiate said instrumentation entity during a post-compile (Improv: pg. 41) model build process, wherein said non-conventional HDL

comment syntax (Bargh: column 27, lines 38-40) is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including (Bargh: column 7,lines 45-50 and 21-24): an input port map field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden (Wu: pg. 78, lines 25-28); and an output port mapping field comprising an override signal (Wu: pg. 78, lines 25-28) field specifying the name of said override signal (Wu: pg. 78, lines 25-28) , a port name field (Bargh: column 7, lines 21-23) specifying the name of the port from which said override signal (Wu: pg. 78, lines 25-28) is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden.

Claim 2. The method of claim 1 wherein said output port mapping (Bargh: column 7,lines 45-50 and 21-24) field further comprises a control port (assumed the ECAC software controls all ports; Bargh: column 7, lines 45-52)) field specifying an output port for delivering an override enable signal to said signal selection means.

Claim 4 The method of claim 2, further comprising instantiating (Bargh: column 7, lines 55-59) a latch within said simulation model, wherein said latch stores an override disable bit; and combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that determines whether of

not said signal selection means overrides said designated signal with said override signal (Wu: pg. 78, lines 25-28).

Claim 5. In a computer-aided design and verification system, a system for facilitating signal override in a simulation model of a digital circuit design) that includes one or more design entities described utilizing a hardware description language (HDL), said system comprising: processing means for instantiating an instrumentation entity (Bargh: column 7, lines 55-59) within at least one or said one or more deign entities using port mapping fields designated by a non-conventional HDL comment syntax (Bargh: column 27, lines 38-40), said non-conventional HDL comment syntax (Bargh: column 27, lines 38-40) processed by a post-compiler (Improv: pg. 41) instrumentation load tool to instantiate said instrumentation entity during a post-compile (Improv: pg. 41) model build process, wherein said non-conventional HDL comment syntax (Bargh: column 27, lines 38-40) is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including: an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and an output port mapping field (Bargh: column 7,lines 45-50 and 21-24) comprising an override signal (Wu: pg. 78, lines 25-28) field specifying the name of said override signal (Wu: pg. 78, lines 25-28), a port name field specifying the name of the port from which said override signal (Wu: pg. 78, lines 25-28) is output from said instrumentation

entity, and a target signal field specifying the name of said designated signal to be overridden.

Claim 6. The system of claim 5, wherein said output port mapping field further comprises a control port (assumed the ECAC software controls all ports; Bargh: column 7, lines 45-52)) specifying an output port for delivering an override enable signal to said signal selection means.

Claim 8. The system of claim 6, further comprising: processing means of instantiating a latch within said simulation model, wherein said latch stores an override disable bit; and processing means for combining said override disable bit with override enable signal within a logic gate to produce a combined selection signal that determines whether or not signal selection means overrides said designated signal with said override signal (Wu: pg. 78, lines 25-28).

Claim 9. In a computer-aided design and verification system, a computer program product of facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said computer program product including computer-executable instructions for performing a method comprising: instantiating (Bargh: column 7, lines 55-59) an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax

(Bargh: column 27, lines 38-40), said non-conventional HDL comment syntax (Bargh: column 27, lines 38-40) processed by a post-compiler (Improv: pg. 41) instrumentation load tool to instantiate said instrumentation entity during post-compile (Improv: pg. 41) model build process, wherein said non-conventional HDL comment syntax (Bargh: column 27, lines 38-40) is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields (Bargh: column 7,lines 45-50 and 21-24) further including: an input mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to overridden; and an output mapping field comprising an override signal (Wu: pg. 78, lines 25-28) specifying the name of said override signal (Wu: pg. 78, lines 25-28), a port name field specifying the name of the port from which said override signal (Wu: pg. 78, lines 25-28) is output from said instrumentation entity, and a target signal field specifying the name of said designated to be overridden.

Claim 10. The computer program product of claim 9, wherein said output port mapping field further comprises a control port (assumed the ECAC software controls all ports; Bargh: column 7, lines 45-52)) field specifying an output port for delivering an overriding enable signal to said selection means.

Claim 12. The computer program product of claim 10, wherein said method further comprises: instantiating a latch within said simulation model, (Bargh: column 24, lines

43-46) wherein said latch stores an override disable bit; and combining said override disable bit with said override enable signal within a logic gate produce a combined selection signal that determines whether of not said signal selection means overrides (Wu: pg. 78, lines 25-28) said designated signal with said override signal (Wu: pg. 78, lines 25-28).

Claim 13. The method of claim 1, further comprising generating signal selection means within said simulation model for selectively overriding said designated signal with said override (Wu: pg. 78, lines 25-28) said responsive to said post-compiler (Improv: pg. 41) instrumentation load tool processing said port mapping fields.

Claim 14. The system of claim 5, further comprising processing means for generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal (Wu: pg. 78, lines 25-28) responsive to said post-compiler (Improv: pg. 41) instrumentation load tool processing said port mapping fields.

Claim 15. The computer program product of claim 9, wherein said method further comprises generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal (Wu: pg. 78, lines 25-28) responsive to said post-compiler (Improv: pg. 41) instrumentation load tool processing said port mapping fields.

Section III: Arguments' Arguments (Final Office Action)

7. Applicants' arguments, see Appeal brief, filed 7/15/05, with respect to the rejection of claims 1,2,4-6,8-10, 12-15 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Wu et al., Bargh et al., and Improv.

Citation of Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- US Patent 6,920,418: The present invention relates in general to designing and simulating digital devices, modules and systems. In particular, the present invention relates to a method and system that improve the model build and simulation processes in order to allow a designer to easily instrument and monitor a simulation model.

- US Patent 6,941,257: A method, system, and data structure for instrumenting a cross-hierarchical simulation event are disclosed herein. The cross-hierarchical simulation event is a function of a first simulation event residing at a first level of simulation model hierarchy and a second simulation event residing at a second level of simulation model hierarchy.

- Darringer et al., "EDA in IBM: Past, Present and Future": Highlight IBM's contributions of multimillion gate ASIC and gigahertz microprocessor design.

- Synopsys, ("Simulation--Tool Invocation Commands" (Oct. 1999)). Discloses a vhdlsim simulator for supporting VHDL delay back annotation using the standard delay format.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

November 18, 2005

TS

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100